3416

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: ZHENG et al.

Docket: VLSI.268PA

Title: ETCH PROCESS THAT RESISTS NOTCHING AT ELECTRODE BOTTOM

CERTIFICATE UNDER 37 CFR 1.10
Express Mail' mailing label number: EL395598528US
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By: Lynda J. Bauer
Name: Lynda J. Bauer

BOX PATENT APPLICATION
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Washington, D.C. 20231

Sir:

We are transmitting herewith the attached:

- ☒ Transmittal sheet containing Certificate under 37 CFR 1.10.
- ☒ Patent Application: Pages Numbered 1-18; 21claims; Abstract 1 pgs.
- ☒ 2 sheets of informal drawings
- ☒ An executed Declaration
- ☒ Assignment of the invention to VLSI Technology, Inc., Recordation Form Cover Sheet
- ☒ Please charge Deposit Account No. 50-0996 (VLSI.268PA) in the amount of $836.00. ($796.00 for the filing fee and $40.00 for the Assignment Recordation Fee.)
- ☒ 1 Return postcard

The fees are calculated as follows:
Basic Filing Fee = $760.00
Fee for total number of claims in excess of 20 = $18 * (22 – 20) = $36.00
Fee for total number of independent claims in excess of 3 = $78 * (3 – 3) = $0
Total fee due = $796.00

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Docket: VLSI.268PA (3416)

ETCH PROCESS THAT RESISTS NOTCHING AT ELECTRODE BOTTOM

Field of the Invention

The present invention is directed generally to a semiconductor method of manufacture, and more particularly to such a method involving plasma etching in the formation of electrodes, such as gate electrodes.

Background of the Invention

The electronics industry continues to strive for high-speed, high-functioning circuits. Significant achievements in this regard have been realized through the fabrication of very large-scale integration of circuits on small areas of silicon wafer. Integrated circuits of this type are manufactured through a series of steps carried out in a particular order. The main objective in manufacturing such devices is to obtain a device which conforms to geographical features of a particular design for the device. To obtain this objective, steps in the manufacturing process are closely-controlled to ensure that rigid requirements, for example, exacting tolerances, quality materials, and clean environment, are realized.

Semiconductor devices are used in large numbers to construct most modern electronic devices. To increase the capability of such electronic devices or to decrease the costs per die in a competitive market, larger numbers of such devices are integrated into a single silicon wafer. As the semiconductor devices are scaled down (*i.e.*, made smaller) to address these needs, the structure of the devices and fabrication techniques

used to make such devices must be refined to remove contaminants and tighten tolerances on acceptable structural imperfections.

A wide variety of processing techniques may be employed in manufacturing silicon integrated circuit devices, such as chips. In those devices, silicon is employed as a semiconductor for conduction of electricity. The chip manufacturing process typically begins with a silicon wafer substrate. The silicon wafer substrate is formed of single-crystal silicon (Si).

Typical steps in the manufacturing process of a silicon integrated circuit device include growing a layer of silicon dioxide (SiO_2, or "oxide") upon the surface of the wafer. Silicon dioxide (or other dielectrics) serves as an insulative material and is often used to separate various semiconducting layers of integrated circuit devices. A variety of methods may be employed to force oxide growth on the wafer, including, for example, thermal oxidation. In thermal oxidation, the silicon reacts with oxygen to form a continuous layer of high-quality silicon dioxide. A film of silicon dioxide can also be formed on the surface of a wafer in other manners. Amorphous or polycrystalline silicon is then deposited on the oxide. For simplicity, these films will be referred to as "polysilicon" here. An organic or inorganic anti-reflective coating (ARC) film may be deposited on top of the polysilicon to improve control of the photolithography process. A variety of techniques, including, for example, photolithography, may be employed to achieve desired wafer surface configurations.

In photolithography, a photoresist material, for example, a photo-sensitive polymer, may be layered atop a somewhat uniform polysilicon or ARC layer on a wafer surface. A mask having a desired design of clear and opaque areas may then be positioned atop the photoresist layer. A resulting characteristic of photoresist response to UV light permits the photoresist to be selectively subjected to UV light and then developed to leave behind an image that will serve as a mask for forming particular patterns of photoresist material atop the polysilicon or ARC. Once a particular pattern of photoresist is formed atop the polysilicon or ARC of a wafer, portions of the wafer topped by polysilicon or ARC but not topped by photoresist may then be etched away from the wafer surface.

Etching is a common procedure employed in manufacture of silicon integrated circuit devices. In general terms, etching is a process by which portions of the wafer surface may be selectively removed from the wafer. The etch process yields a layer on the wafer surface having a desired geographical arrangement for further processing. After the etch, the photoresist is removed by a subsequent processing step, leaving the silicon wafer topped only by select configurations of polysilicon or ARC.

The general silicon dioxide/polysilicon/ARC/photoresist/etch method described above is often used in the formation of the gate electrode portion of a transistor. Such gate electrode formation involves layering an oxide, followed by a conductive polysilicon layer, over the underlying (typically doped) silicon used to form the active and isolation regions. The portions of the conductive polysilicon layer designated to form the

resultant gate electrodes are hardmasked, for example, using SiON. Gate electrodes are then formed by selectively etching the conductive polysilicon in such a manner that trenches are formed between adjacent gate electrodes. Selectively etching in this context refers to etching the unmasked material, thereby providing a trench with substantially vertical sidewalls.

The ideal selective etching process would provide perfectly vertical sidewalls that provide an interface at the trench bottom which is normal. In practice, however, process changes made to increase silicon-to-oxide selectivity result in notching at the bottom of the gate electrode. FIG. 1 illustrates this notching effect at the bottom of the pillar-like electrode structures.

In modern semiconductor applications, the thickness of the underlying layer of gate oxide has been reduced to about 30 Å for 0.15 micron and similar technologies. In the future, the gate oxide layer will be thinned further, perhaps to as little as 15-20 Å. Due to the notching problem described above, the plasma etch process conventionally used to define the gate electrode inevitably consumes some of this oxide; consequently, process changes are made to boost silicon-to-oxide selectivity to minimize the loss. In the prior art, changes such as reducing bias power have been found to be useful for improving selectivity, but with the disadvantage of lateral etching beginning to occur as the sidewall protection of the gate electrode is diminished. This lateral etching typically appears as a notch at the gate/oxide interface.

Accordingly, there is a need to improve the process of forming the gate electrode in a manner that overcomes the aforementioned deficiencies.

Summary of the Invention

Generally, the present invention relates to a semiconductor device manufactured using a more accurate gate-electrode formation process. Consistent with the present invention, a semiconductor device is formed as part of a wafer having an upper surface, with at least one device layer over the upper surface of the wafer. The device layer is formed using a silicon-to-oxide selectivity during gate etch to improve sidewall protection and to eliminate notching at the bottom of the gate electrode. In connection with the one embodiment of the present invention, it has been discovered that adding a small amount of nitrogen during the endpoint step prevents the notch without affecting selectivity. A more specific embodiment of the present invention provides a method for improving sidewall protection and preventing notch formation without affecting silicon:oxide selectivity. During the endpoint step, a small amount of nitrogen is added to the conventional polysilicon etch chemistry.

In accordance with another embodiment of the present invention, a process of forming a semiconductor device, includes: forming at least one device layer over a wafer surface; providing a mask over a portion of the device layer; using a plasma-etch and selective etching into the device layer to form a pillar structure having at least one sidewall, the selective etching includes the use of nitrogen as part of the plasma etch.

Yet another embodiment of the present invention is directed to a process of forming a semiconductor device, comprising: forming at least one device layer over an underlying dielectric layer, the device layer and the underlying dielectric layer being over a wafer surface; providing a mask over a portion of the device layer; a step of using a plasma-etch of a first chemistry and selectively etching into the device layer for a function of forming a pillar structure having at least one sidewall. After the step of using the first chemistry, using a step of using a plasma-etch of a different second chemistry that includes less than about ten percent nitrogen of gas flow in the second chemistry for a function of completing the selective etching upon etching up to the underlying dielectric layer. In another embodiment, the second chemistry includes less than about five percent of the gas flow.

In another embodiment, a process of forming a semiconductor device includes forming at least one gate electrode layer over a gate oxide; providing a hardmask over a portion of the device layer; using a plasma-etch of a first chemistry that includes HBr and selectively etching into the device layer to form a pillar structure having at least one sidewall. After using the first chemistry, a plasma-etch of a different second chemistry that includes HBr and nitrogen and selectively etching into the device layer to form a pillar structure having at least one sidewall is used. The second chemistry includes using nitrogen in an amount less than about ten percent of gas flow of the second chemistry and terminating the use of a plasma-etch of the second chemistry in response to reaching

the gate oxide. The first chemistry can include HBr/ Cl_2, HBr/HCl, or HBr/ Cl_2/ Cl_4 for etching through the polysilicon, and can also include a selectivity booster such as He-O_2.

The above summary of the present invention is not intended to describe each illustrated embodiment or every implementation of the present invention. The figures and the detailed description which follow more particularly exemplify these embodiments.

Brief Description of the Drawings

The invention may be more completely understood in consideration of the following detailed description of various embodiments of the invention in connection with the accompanying drawings, in which:

FIG. 1 illustrates an actual cross-sectional view of a conventional semiconductor device in which gate electrode lines illustrate the notching issue addressed by the present invention;

FIG. 2 illustrates a cross-sectional sketch of a semiconductor device in which gate electrode lines are formed in accordance with an example embodiment of the present invention; and

FIG. 3 illustrates an actual cross-sectional view of a semiconductor device in which gate electrode lines are formed in accordance with an example embodiment of the present invention.

While the invention is amenable to various modifications and alternative forms, specifics thereof have been shown by way of example in the drawings and will be described in detail. It should be understood, however, that the intention is not to limit the invention to the particular embodiments described. On the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

Detailed Description of Various Embodiments

The present invention is believed to be applicable to a number of semiconductor devices which are manufactured using an electrode etching process. The invention has been found to be particularly advantageous in application environments where it is desirable to form gate electrodes over gate oxide layers that are relatively thin, for example, less than about 50 Å, and in other applications, less than about 30 Å. For further reductions in thickness of the gate oxide layer, the recognizable contributions in using various embodiments of the present invention increase significantly. While the present invention is not necessarily limited to any particular applications of this type, an appreciation of various aspects of the invention is best gained through a discussion of various application examples of processes used to form such semiconductor devices.

Generally, the exemplary processes discussed below illustrate a variety of techniques for forming a semiconductor device in which a polysilicon gate electrode is formed over a thin underlying dielectric layer, such as a gate oxide, using a plasma etch process that significantly retards notching as the plasma etch approaches the endpoint, *i.e.*, the thin underlying dielectric layer. According to one embodiment, a plasma etching process used to form the gate electrode includes includes a plasma containing a selected amount of nitrogen in the overall gas flow to provide a desired retardation of notching near the thin underlying dielectric layer.

Referring to FIG. 2, a cross-sectional view of a portion of a semiconductor device 10 shows polysilicon gate electrodes at lines 20 between an overlying hardmask 22 and an underlying dielectric layer 24 such as an oxide. The dielectric layer 24 resides over a silicon wafer region 26 that is used in forming the source/drain and channel regions (not shown) of the transistors including the gate electrodes 20. The gap between the gate electrodes 20 is a trench formed using a plasma etch chemistry that provides little if any notching at the trench bottom.

In one particular example application, two different plasma chemistries are used to retard the notching effect at the bottom of the trench. The first chemistry is a conventional chemistry for selectively etching into the gate electrode material and not into the mask atop the gate electrode material. For example, using a hardmask such as SiON, the first chemistry can include HBr/ Cl_2, HBr/HCl, or HBr/ Cl_2/ Cl_4, for selectively etching a polysilicon electrode material. The first chemistry can also include a selectivity

booster such as $He-O_2$. After using the first chemistry and sometime before reaching the underlying gate oxide, the chemistry is changed to one that includes a small amount of nitrogen, *e.g.*, less than about twelve to fifteen percent of gas flow in the second chemistry depending on the application. This second chemistry is used to complete the selective etching, with an endpoint detection process or other technique used to terminate this nitrogren-modified plasma etch. By adding such an amount of nitrogen before the endpoint termination, the notching effect such as shown in FIG. 1 is avoided without affecting the selectivity of the overall etching process.

In another particular example application, the same plasma chemistry is used in the trenching to form the electrode pillar, wherein the benefit of the added nitrogen to retard the notching effect at the bottom of the trench is realized when the etching approaches the underlying electrode dielectric. Any of the so-called second chemistries, discussed herein, can be used in this process.

Accordingly, an important aspect of the present invention is the use of a small amount of nitrogen in completing the plasma etching for formation of the gate electrode. In one embodiment, this plasma etching includes using less than about ten percent of nitrogen in the plasma chemistry when etching near the underlying electrode dielectric. For other applications, this amount of nitrogen can vary depending upon the desired need for retarding the notching effect and/or minimizing any adverse effect on overall selectivity.

FIG. 3 illustrates an actual cross-sectional view of a semiconductor device in which gate electrode lines are formed, according to an example embodiment of the present invention, using nitrogen in an amount of about two percent (specifically, 1.7 percent) of the total plasma gas flow. In this example embodiment, the silicon etching tool being used is a Lam Research Corp. TCP 9400SE silicon etch tool, and using SiON as a hardmask atop the portions of the polysilicon to be used in forming the pillar electrode structures. For reliable control of such low flow rates, rather than using a pure N_2 as the nitrogren additive, a diluted gas mixture such as 80% helium/20% nitrogen (He-N_2), may be advantageous.

The amorphous silicon and thermal oxide etch rates and selectivities with and without nitrogen are shown below in Table I using photoresist-patterned wafers for measurements. Nitrogen addition has a small impact with the difference (*e.g.*, 5% or less) well within the measurement error, and on hardmasked wafers, the oxide etch rate is so low that it is not measurable, giving nearly infinite selectivity.

Table I. Etch rate and selectivity measurements.

	No N_2 added	With 20 sccm N_2	Delta (%)
Amorphous silicon etch rate (Å/sec)	17.9	18.1	-1%
Thermal oxide etch rate (Å/sec)	0.44	0.46	-5%
Silicon:oxide selectivity	40.7	39.3	3%

The following Table II exemplifies an acceptable chemistry for achieving the formation of the electrode structure illustrated in FIG. 3:

Hard mask gate etching with N2 addition at end point step								
		Breakthrough		Bulk Endpoint		Over Etch		
	Step 01	Step 02	Step 03	Step 04	Step 05	Step 06	Step 07	Step 08
Pressure (mT)	10.00	10.00	20.00	20.00	80.00	80.00	90.00	0.00
RF-Top (W)	0.0	350.0	0.0	150.0	0.0	250.0	0.0	0.0
RF-Bottom (W)	0.0	50.0	0.0	30.0	0.0	70.0	0.0	0.0
Gap (cm)	8.100	8.100	8.100	8.100	8.100	8.100	8.100	8.100
Cl2 (sccm)	0.0	0.0	10.0	10.0	0.0	0.0	0.0	0.0
HBr (sccm)	0.0	0.0	150.0	150.0	200.0	200.0	0.0	0.0
80%He-O2 (sccm)	0.0	0.0	15.0	15.0	10.0	10.0	0.0	0.0
CF4 (sccm)	100.0	100.0	0.0	0.0	0.0	0.0	0.0	0.0
He (sccm)	0.0	0.0	0.0	0.0	200.0	200.0	200.0	0.0
N2 (sccm)	0.0	0.0	3.0	3.0	0.0	0.0	0.0	0.0
He clamp (T)	8.0	8.0	8.0	8.0	8.0	8.0	0.0	0.0
Completion	Stabl	Time	Stabl	EndPt	Stabl	Time	Time	End
Time	30	8	30	150	30	60	7	
Channel				A				
Delay (sec)				40				
Norm (sec)				1				
Trigger (%)				99				

Temperatures	(°C)
Bottom Electrode	65.0
Chamber	60.0

Channel	Wavelength (nm)
A	405
B	520

MFC	Gas	sccm
1	Cl2	200
2	HBr	200
3	80%He-O2	20
4	CF4	200
5	He	200
6	SF6	100
7	O2	100
8	N2	50

The present invention is applicable to fabrication of various types of electrodes having an underlying thin dielectric layer that reacts to the nitrogen plasma additive in the same manner as oxide. The present invention should not be considered limited to the particular examples described above, but rather should be understood to cover all aspects of the invention as fairly set out in the attached claims. Various modifications, as well as numerous structures to which the present invention may be applicable, will be readily apparent to those of skill in the art upon review of the present specification. The claims are intended to cover such modifications and devices.

What is Claimed is:

1. A process of forming a semiconductor device, comprising:

forming at least one device layer over a wafer surface;

providing a mask over a portion of the device layer;

using a plasma-etch and selectively etching into the device layer to form a pillar structure having at least one sidewall, the selective etching including use of nitrogen as part of the plasma etch.

2. A process of forming a semiconductor device, according to claim 1, wherein the second chemistry includes nitrogen in an amount less than about ten percent of gas flow in the second chemistry.

3. A process of forming a semiconductor device, according to claim 1, wherein the second chemistry includes nitrogen in an amount less than about two percent of gas flow in the second chemistry.

4. A process of forming a semiconductor device, according to claim 1, wherein the second chemistry includes nitrogen in an amount less than about ten percent of gas flow in the second chemistry, and wherein the second chemistry includes a diluted gas mixture of nitrogen.

5. A process of forming a semiconductor device, according to claim 1, wherein the device layer is polysilicon, and the second chemistry includes in an amount less than about ten percent of gas flow in the second chemistry.

6. A process of forming a semiconductor device, according to claim 5, wherein the mask is a hardmask, and the first chemistry includes one of HBr/ Cl_2, HBr/HCl, or HBr/ Cl_2/ Cl_4.

7. A process, according to claim 6, wherein the first chemistry further includes the first chemistry also includes a selectivity booster.

8. A process of forming a semiconductor device, comprising:

forming at least one device layer over an underlying dielectric layer, the device layer and the underlying dielectric layer being over a wafer surface;

providing a mask over a portion of the device layer;

a step of using a plasma-etch of a first chemistry and selectively etching into the device layer for a function of forming a pillar structure having at least one sidewall; and

after the step of using the first chemistry, using a step of using a plasma-etch of a different second chemistry that includes less than about ten percent nitrogen of gas flow in the second chemistry for a function of completing the selective etching upon etching up to the underlying dielectric layer.

9. A process, according to claim 8, wherein the device layer includes at least one of: a layer of polysilicon; and an anti-reflective coating on a layer of polysilicon.

10. A process, according to claim 8, wherein the device layer is polysilicon and the pillar structure is a gate electrode.

11. A process, according to claim 10, wherein the mask is a hardmask.

12. A process, according to claim 11, wherein the mask is formed using SiON.

13. A process, according to claim 12, wherein the first chemistry includes HBr/Cl_2. and a selectivity booster.

14. A process, according to claim 12, wherein the first chemistry includes at least one of HBr/Cl_2 and $HBr/ Cl_2/ Cl_4$

15. A process, according to claim 14, wherein the second chemistry includes nitrogen in an amount less than about ten percent of gas flow in the second chemistry, and wherein the second chemistry includes a diluted gas mixture of nitrogen.

16. A process, according to claim 8, wherein the second chemistry includes nitrogen in an amount less than about two percent of gas flow in the second chemistry.

17. A process, according to claim 8, wherein the second chemistry includes nitrogen in an amount less than about ten percent of gas flow in the second chemistry.

18. A process of forming a semiconductor device, comprising:

forming at least one gate electrode layer over a gate oxide, the gate oxide being above a wafer surface;

providing a hardmask over a portion of the device layer;

using a plasma-etch of a first chemistry that includes HBr and selectively etching into the device layer to form a pillar structure having at least one sidewall;

after using the first chemistry, using a plasma-etch of a different second chemistry that includes HBr and nitrogen and selectively etching into the device layer to form a pillar structure having at least one sidewall, the second chemistry including nitrogen in an amount less than about ten percent of gas flow of the second chemistry; and

terminating the use of a plasma-etch of the second chemistry in response to reaching the gate oxide.

19. A process, according to claim 18, wherein the first chemistry includes one of HBr/ Cl_2, HBr/HCl, or HBr/ Cl_2/ Cl_4, and also includes a selectivity booster.

20. A process, according to claim 18, wherein the first chemistry includes HBr/ Cl_2 and He-O_2.

21. A process, according to claim 18, wherein the second chemistry includes a diluted gas mixture of nitrogen.

Abstract

A semiconductor device is manufactured using a small amount of nitrogen in the gate electrode etch process to minimize notching at the bottom of the electrode. Consistent with one embodiment of the present invention, the gate electrode etch process includes using a plasma-etch and selectively etching into the device layer to form the electrode with its lower sidewalls protected using a relatively small percentage of nitrogen in the plasma gas flow.

FIG. 1

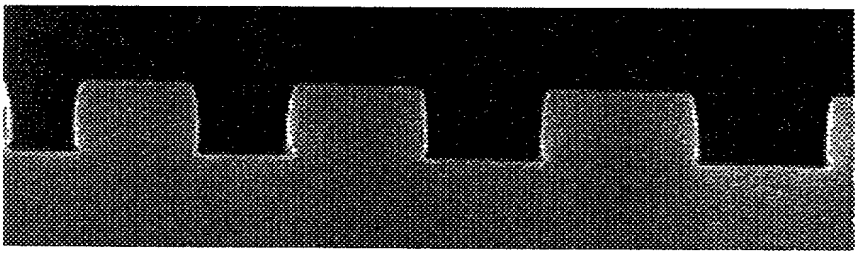


FIG. 3

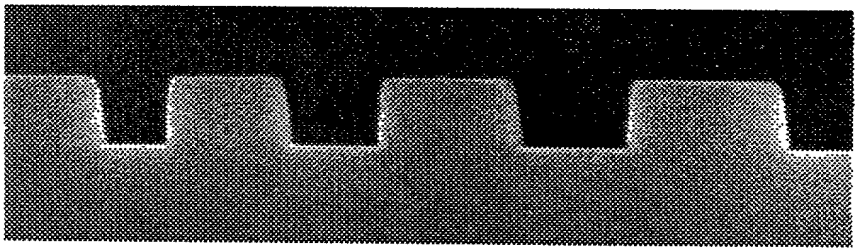
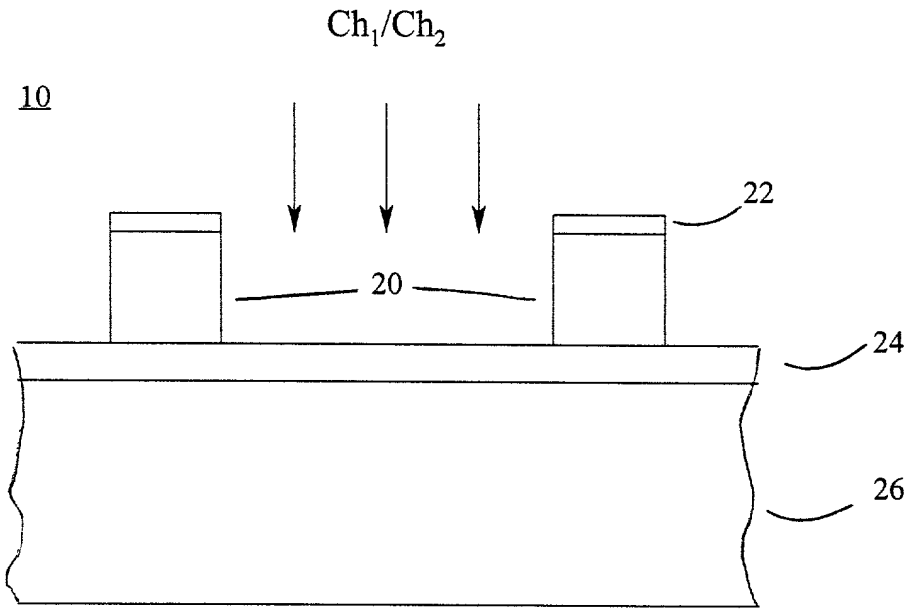


FIG. 2



Docket No. VLSI.268PA (3416)

CRAWFORD PLLC

United States Patent Application

DECLARATION UNDER 37 C.F.R. § 1.63

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **ETCH PROCESS THAT RESISTS NOTCHING AT ELECTRODE BOTTOM.**
The specification of which
a. ☒ is attached hereto
b. ☒ is entitled **ETCH PROCESS THAT RESISTS NOTCHING AT ELECTRODE BOTTOM**, having attorney docket number VLSI.268PA.
c. ☐ was filed on as application serial no. and was amended on (if applicable) (in the case of a PCT-filed application) described and claimed in international no. filed and as amended on (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

a. ☒ no such applications have been filed.
b. ☐ such applications have been filed as follows:

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC § 119			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)
ALL FOREIGN APPLICATION(S), IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

U.S. PROVISIONAL APPLICATION NUMBER	DATE OF FILING (Day, Month, Year)

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/ organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Crawford PLLC to the contrary.

Please direct all correspondence in this case to Crawford PLLC at the address indicated below:

Crawford PLLC
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief ar believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2 0 1	**Full Name Of Inventor**	**Family Name** ZHENG	**First Given Name** TAMMY	**Second Given Name**
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Signature of Inventor 201: Tammy Zheng			**Date:** 1 NOV, 1999	
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Signature of Inventor 202: Calvin Todd Gabriel			**Date:** 1 Nov 1999	
2 0 3	**Full Name Of Inventor**	**Family Name**	**First Given Name**	**Second Given Name**
	Residence & Citizenship	**City**	**State or Foreign Country**	**Country of Citizenship**
	Post Office Address	**Post Office Address**	**City**	**State & Zip Code/Country**
Signature of Inventor 203:			**Date:**	
2 0 4	**Full Name Of Inventor**	**Family Name**	**First Given Name**	**Second Given Name**
	Residence & Citizenship	**City**	**State or Foreign Country**	**Country of Citizenship**
	Post Office Address	**Post Office Address**	**City**	**State & Zip Code/Country**
Signature of Inventor 204:			**Date:**	

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability o any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated wit the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.